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TITLE OF INVENTION: A RECONFIGURABLE TOPOLOGY FOR SWITCHING AND LINEAR VOLTAGE REGULATORS	
TI FILE NO.: TI-35749	DEPOSIT ACCT. NO.: 20-0668
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JAN 17 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Trafton

Docket No: TI-35749

Serial No: 10/646,854


Examiner: Laxton, Gary L.

Filed: 8/26/2003

Art Unit: 2838

For: A RECONFIGURABLE TOPOLOGY FOR SWITCHING AND LINEAR VOLTAGE
REGULATORSAPPEAL BRIEF PURSUANT TO 1.192(c)Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

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The following Appeal Brief is respectfully submitted in connection with the above identified application in response to the final rejection mailed January 27, 2005, the Advisory Action mailed April 20, 2005, and the Notice of Non Compliance mailed November 17, 2005.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

RELATED APPEALS AND INTERFERENCES

Appellants legal representative knows of no appeals or interferences which will be directly affected, or have a bearing on the Board's decision.

TI-35749 Page 1

STATUS OF THE CLAIMS

Claims 1-19 were originally filed with Claim 13 being subsequently claimed.

Claims 5-10 and 14-19 have been allowed. Thus, the subject matter of the instant appeal is Claims 1-4, 11, and 12.

STATUS OF AMENDMENTS

A Response after final action was filed, amending no claims. Thus, the subject matter of the instant appeal is Claims 1-4, 11, and 12.

SUMMARY OF THE CLAIMED SUBJECT MATTER

Referring first to Figure 2, integrated circuit 20 according to the preferred embodiment of the invention will now be described. Integrated circuit 20, in this example, includes functional circuitry 22 for performing a particular device function, and also includes voltage regulator 28 constructed according to the preferred embodiment of the invention. Functional circuitry 22 is logic or other circuitry for performing a desired electronic function, and will be connected to various input, output, and input/output terminals (not shown) of integrated circuit 20 in order to effect that function. Of course, functional circuitry 22 may include such circuitry as used to perform any function suitable for realization in an integrated circuit, and as such the various circuitry implemented within functional circuitry 22 may vary widely. Further in the alternative, functional circuitry 22 may be omitted from integrated circuit 20, for example where the entire function of integrated circuit 20 is a voltage regulator or voltage converter, for example if the function of integrated circuit 20 is to control the power supply of a computer disk drive. It is contemplated that those skilled in the art having reference to this specification will be readily able to implement this invention within an integrated circuit of any function desired.

According to the preferred embodiment of the invention shown in Figure 2, voltage regulator 28 in integrated circuit 20 is connected to several external terminals DRV, SENS1, SENS2, SENS3. As will become apparent from the following description, voltage regulator 28 drives an external pass or switching transistor from terminal DRV, while terminals SENS1, SENS2, SENS3 provide feedback to voltage regulator 28, and also configure its mode of operation, which in this embodiment of the invention, can be either as a linear regulator or a switching regulator. Alternatively, voltage regulator 28 may be configured by writing to a register, or by way of logic circuitry responsive to program or user control, or further in the alternative may operate according to different voltage regulator topologies.

In this preferred embodiment of the invention, voltage regulator 28 includes error amplifier 36, which is used in each of the two operating configurations. Error amplifier 36 is a conventional differential amplifier, biased in the conventional manner (not shown), including feedback capacitor 36C connected between its output and its non-inverting input. The non-inverting input of error amplifier 36 also receives a reference voltage generated by bandgap reference circuit 24, which is a conventional circuit for generating a reference voltage that is stable over temperature and power supply voltage variations, as known in the art. Bandgap reference circuit 24 is illustrated as implemented outside of voltage regulator 28, in this embodiment of the invention, considering that its output reference voltage may also be used elsewhere within integrated circuit 20. The reference voltage from bandgap reference circuit 24 is preferably coupled to error amplifier via soft-start circuit 32 in voltage regulator 28. Soft-start circuit 32 is a conventional circuit for ramping the application of the reference voltage from bandgap reference circuit 24 to error amplifier 36, such as during startup or reset of integrated circuit 20, so that the output regulated voltage also ramps up during that time, to avoid output current spikes.

Error amplifier 36 has an output that is connected to the pole of switch 34B. Switch 34B has two throws, one connected to an inverting input to differential amplifier 42B, and the other connected to one of the throws of switch 34A. The pole of switch 34A is connected to gate driver 35, which drives terminal DRV at the output of voltage

regulator 28, from a bias voltage VM. The other throw of switch 34A is driven by the output of one shot multivibrator 46, and as such switch 34A selects the circuit element within voltage regulator 28 that drives gate driver 35. Switches 34A, 34B are controlled by the output of configuration amplifier 40, which is a differential amplifier having a fixed voltage at its non-inverting input, and terminal SENS1 at its inverting input. The fixed voltage applied to the non-inverting input, according to this embodiment of the invention, is power supply voltage V_{cc} less a diode drop (V_t), as shown in Figure 2. Configuration amplifier 40 controls the state of switches 34A, 34B in response to the comparison between the voltage at terminal SENS1 and the fixed voltage (e.g., power supply voltage V_{cc} less V_t), and thus sets the operating mode of voltage regulator 28, as will be described in further detail below.

Switches 34A, 34B are preferably implemented as pass transistors, implemented in the particular technology (bipolar, MOS, BiCMOS, or the like) according to which the remainder of integrated circuit 20 is constructed. For example, each of switches 34A, 34B may be easily implemented in the form of complementary MOS pass transistors, in the case where functional circuitry 22 is constructed according to CMOS technology. It is contemplated that those skilled in the art having reference to this specification will be readily able to implement configuration switches 34A, 34B in an efficient manner for the particular technology involved in the remainder of integrated circuit 20.

In addition, while a pair of configuration switches 34A, 34B are illustrated in this embodiment of the invention, it is of course contemplated that a different number of configuration switches may be used, depending upon the particular arrangement of the elements of voltage regulator 28. For example, it is contemplated that a single configuration switch may be useful in some realizations, while three or more switches may be used in other realizations.

As mentioned above, the inverting input of differential amplifier 42B is connected to a throw of switch 34B; the non-inverting input of differential amplifier 42B is connected to terminal SENS2, as is the non-inverting input of differential amplifier 42A. The inverting input of differential amplifier 42A is coupled to terminal SENS2 through

voltage source 38. The outputs of amplifiers 42A, 42B are connected to inputs of logic function 44, which has its output connected to one-shot multivibrator 46. In this preferred embodiment of the invention, one-shot multivibrator 46 is a constant off-time one-shot, generating a high logic level output except when triggered by a pulse at its input. As known in the art, the constant off-time one-shot multivibrator maintains its output low for a specified time after the end of the triggering pulse at its input. Accordingly, logic function 44 in this example is an OR gate. As mentioned above, the output of constant off-time one-shot multivibrator 46 is selectably coupled to the control input of gate driver 35 through switch 34A.

In operation, according to this preferred embodiment of the invention, voltage regulator 28 is configured by the voltage at external terminal SENS1, and specifically according to whether the voltage at external terminal SENS1 exceeds or falls below the fixed voltage at the non-inverting input of configuration amplifier 40. In addition, the system implementer will connect the appropriate external components to terminals DRV, SENS1, SENS2, SENS3 for the selected voltage regulator configuration. Figures 3a and 3b illustrate the configuration of voltage regulator 28 as linear and switching regulators, respectively, as will now be described.

Referring now to Figure 3a, voltage regulator 28 is shown in its linear regulator configuration. As mentioned above, the fixed voltage applied to the non-inverting input of configuration amplifier 40 is at least a diode voltage drop (V_D) below power supply voltage V_{CC} . Accordingly, in this embodiment of the invention, the linear amplifier mode is selected by the biasing of external terminal SENS1 to power supply voltage V_{CC} , as shown in Figure 3. This biasing causes configuration amplifier 40 to control switches 34A, 34B to connect the output of error amplifier 36 to the input of gate driver 35, as shown in the example of Figure 3a. This configures voltage regulator 28 as a linear regulator.

The external components to voltage regulator 28 in its linear regulator configuration include n-channel MOS pass transistor 50, which has its drain connected to power supply voltage V_{CC} (or to a higher power supply voltage than power supply

voltage V_{cc} , if desired). Pass transistor 50 has its gate driven from terminal DRV at the output of gate driver 35. The source of pass transistor 50 is connected to one end of a series path through resistors 52, 54 to ground. Output terminal V_{out} is at the voltage divider node between resistors 52, 54, and output capacitor 56 is connected between output terminal V_{out} and ground. It is contemplated that those skilled in the art having reference to this specification will be able to readily select the parameters and values of each of these external devices, including pass transistor 50, resistors 53, 54, and capacitor 56. External terminal SENS3 of voltage regulator 28 (and integrated circuit 20) is connected to output terminal V_{out} . External terminal SENS2 of voltage regulator 28 is not used in this configuration, and is simply left open.

In operation as a linear regulator, the voltage at output terminal V_{out} and at external terminal SENS3 is applied to the inverting input of error amplifier 36, which compares this voltage to the bandgap reference voltage at the non-inverting input of error amplifier 36. In this configuration, switches 34A, 34B directly connect the output of error amplifier 36 to gate driver 35. If the voltage at output terminal V_{out} is below the bandgap reference voltage, error amplifier 36 issues a positive polarity voltage at its output, which causes gate driver 35 to turn on external pass transistor 50. With pass transistor 50 on, output terminal V_{out} is charged from power supply voltage V_{cc} . Upon the voltage at output terminal V_{out} exceeding the bandgap reference voltage, error amplifier 36 then issues a negative polarity output to gate driver 35, causing it to turn off external pass transistor 50. Upon the voltage at output terminal V_{out} then falling below that of the band gap reference voltage, error amplifier 36 causes gate driver 35 to again turn on pass transistor 50, and the process repeats. In this manner, voltage regulator 28 operates as a feedback control linear voltage regulator, driving output terminal V_{out} to a voltage matching its reference voltage (e.g., the bandgap reference voltage produced by bandgap reference circuit 24).

Referring now to Figure 3b, the configuration and operation of voltage regulator 28 as a switching regulator of the constant off-time "Buck" mode type, will now be described. As known in the art, various configurations of switching regulators may be used, depending on the voltage required, and also the desired manner of regulation.

Conventional classes of switching regulators include "Buck" regulators of various types, "Boost" regulators, "Boost-Buck" regulators, and "flyback" switching regulators, for example. Accordingly, the configuration of voltage regulator 28 as illustrated in Figure 3b is provided by way of example only, and is not intended to limit the scope of the invention as claimed.

In this example, external n-channel MOS switching transistor 60 has its gate connected to terminal DRV, which is driven by gate driver 35 of voltage regulator 28 as described above. The drain of switching transistor 60 is biased to power supply voltage V_{cc} , and its source is connected to one end of external inductor 61. A network of capacitor 67 and diode 68 is connected in parallel with the drain-to-source path of switching transistor 60, with the anode of diode 68 at its connection to capacitor 67 tied to ground.

Inductor 61 is connected in series between the source of switching transistor 60 and resistor 62. The node at the connection between inductor 61 and resistor 62 is connected also to terminal SENS1 of integrated circuit 20, which is connected to the inverting input of configuration amplifier 40 and the non-inverting inputs of differential amplifiers 42A, 42B. Resistor 62 is in an R-C network that defines the voltage at output terminal V_{out} , at a node between resistor 62 and one plate of output capacitor 66, which has its other plate at ground; this node is also connected to terminal SENS2, and thus to the inverting input of differential amplifier 42A via voltage source 38. Resistor 64 is in series with resistor 65 in a path between output terminal V_{out} and ground. The voltage divider node between resistors 64 and 65 is connected to terminal SENS3, and thus to the inverting input of error amplifier 36 in voltage regulator 28.

The configuration of voltage regulator 28 as a switching regulator is effected by terminal SENS1 being below the fixed voltage applied to the non-inverting input of configuration amplifier 40. In the preferred embodiment of the invention, the fixed voltage is set at a diode drop, or threshold voltage, below power supply voltage V_{cc} (i.e., $V_{cc} - V_t$). In the configuration of Figure 3a, terminal SENS1 will necessarily be no higher than this fixed voltage, because switching transistor 60 is n-channel, and

assuming that the output of gate driver 35 will not exceed power supply voltage V_{cc} (because its bias voltage V_M is below V_{cc}). This bias ensures that the source of transistor 60 cannot rise above a threshold voltage lower than its drain voltage, which is at power supply voltage V_{cc} . Accordingly, the output of configuration amplifier 40 causes switch 34A to connect gate driver 35 to the output of constant off-time one-shot multivibrator 46, and causes switch 34B to connect the output of error amplifier 36 to the inverting input of differential amplifier 42B.

Differential amplifiers 42A, 42B are thus enabled to respond to the voltages at terminals SENS2, SENS3, respectively. The voltage at terminal SENS2 is increased by voltage source 38, for example increased by a small amount such as 0.3 volts, and the increased voltage is applied to the inverting input of differential amplifier 42A for comparison against the voltage at terminal SENS1. Accordingly, differential amplifier 42A determines whether the voltage drop across resistor 62 exceeds the voltage of voltage source 38, which in effect determines whether the load current through inductor 61 exceeds a predetermined threshold defined by the resistance of resistor 62 and the voltage of voltage source 38. As such, differential amplifier 42A operates as a current limiter. On the other hand, error amplifier 36 outputs a voltage corresponding to the difference between the voltage at terminal SENS3, at the node between resistors 64, 65, and the bandgap reference voltage. The error voltage output from error amplifier 36 is thus an indication of the output voltage at output terminal V_{out} . Differential amplifier 42B effectively compares the error voltage output against the voltage at terminal SENS1, and provides this result to logic function 44, which in turn controls constant off-time one-shot multivibrator 46. As such, differential amplifier 42B effectively controls the output voltage at output terminal V_{out} , as will now be described.

In operation, voltage regulator 28 begins charging output terminal V_{out} from a low voltage near ground. Initially, the voltage at terminal SENS3 is below the bandgap reference voltage (as presented by soft-start circuit 32). The relatively large positive polarity error voltage from error amplifier 36 results in differential amplifier 42B presenting a low voltage to OR function 44. This low level input to OR function 44, along with the initial low output of differential amplifier 42A from the initial low output

current, applies a low level input to constant off-time one-shot 46, maintaining the output of constant off-time one-shot 46 at a high level, which is passed through configuration switch 34A to gate driver 35. Gate driver 35 thus drives transistor 60 to an on-state, passing current through inductor 61 to charge capacitor 66, and raising the voltage at output terminal V_{out} . In this embodiment of the invention, prior to the voltage at output terminal V_{out} reaching its regulated voltage, the charging current conducted through transistor 60 and inductor 61 typically increases enough that the voltage drop across resistor 62 exceeds that of voltage source 38; in this event, the state of differential amplifier 42A will switch, presenting a high logic level to OR function 44, and presenting a high logic level pulse to constant off-time one-shot 46. This causes constant off-time one-shot 46 to de-energize its output, which turns off gate driver 35 and transistor 60. The current conducted by inductor 61 will continue at least instantaneously (via diode 68), then decaying so that the voltage drop across resistor 62 drops below the voltage of voltage source 38, at which time the output of differential amplifier 42A goes low, ceasing the high level pulse at the output OR gate 44 that is presented to constant off-time one-shot 46. Upon the output of OR gate 44 going low again, but after the constant off-time period elapses, constant off-time one-shot 46 then again energizes its output to turn on gate driver 35, which in turn turns on transistor 60, until the voltage drop across resistor 62 again exceeds that of voltage source 38. This sawtooth operation continues until the voltage at output terminal V_{out} approaches the desired regulated voltage, at which point the current conducted through inductor 61 and resistor 62 remains relatively small, at which time the voltage drop across resistor 62 remains small and no longer controls the operation of voltage regulator 28, absent any large event (e.g., a change in the load, a reset event, or the like).

The voltage at output terminal V_{out} determines the voltage at terminal SENS3, which is measured against the bandgap reference voltage by error amplifier 36 and, once sufficiently charged, controls the operation of voltage regulator 28, as will now be described. When the voltage at terminal SENS3 exceeds the bandgap reference voltage, error amplifier 36 produces a negative voltage that, in turn, causes error amplifier 42B to issue a positive polarity level to OR function 44. OR function 44 in turn

presents a high level at the input to constant off-time one-shot 46, which turns off the output of constant off-time one-shot 46 and thus turns off gate driver 35 and transistor 60. The current through inductor 61 remains instantaneously constant through the operation of diode 68, after transistor 60 turns off, and the voltage at output terminal V_{out} instantaneously remains at its same level. Eventually, however, the voltage at output terminal V_{out} and thus at terminal SENS3 begins to decay, as does the current through inductor 61. Upon the sensed voltage at terminal SENS3 falling below the bandgap reference voltage, error amplifier 36 produces a negative polarity output, causing differential amplifier 42B to generate a negative output, which causes OR gate 44 to present a low level input at the input to constant off-time one-shot 46. After the constant off-time elapses, constant off-time one-shot 46 then again turns on gate driver 35, turning on transistor 60, which pulls up output terminal V_{out} , again until the voltage at terminal SENS3 reaches the bandgap reference voltage as measured at error amplifier 36, at which time the process repeats. Voltage regulator 28 continues to operate in this manner, thus presenting a stable regulated voltage at output terminal V_{out} .

Voltage regulator 28 is thus able to operate either as a switching regulator, as shown in the configuration of Figure 3b, or as a linear regulator, as shown in the configuration of Figure 3a. According to this embodiment of the invention, therefore, the same integrated circuit may include voltage regulators of different topologies, with the selection of the regulator topology readily made by the manner in which the integrated circuit is implemented into its system or end equipment. The system integrator using the integrated circuit according to this embodiment of the invention is therefore able to utilize the same integrated circuit in different implementations, without requiring separate manufacturing inventory of the integrated circuits itself. This important ability is attained, according to this invention, in a manner that is especially efficient, considering that the different voltage regulator topologies are able to share significant portions of the voltage regulator circuitry, especially large devices in terms of chip area such as the error amplifier and the feedback capacitor for the error amplifier. In addition, external terminals and internal conductors to those terminals are also

shared by the available voltage regulator topologies, implementing still further efficiency in the resulting device, especially in very large scale integrated circuits that have many terminals, and for which additional external terminals are quite costly.

As mentioned above, the foregoing example illustrates a voltage regulator that can be configured as either a linear regulator or a Buck type switching regulator. According to this invention, other types of regulators may similarly be implemented within the same integrated circuit, also sharing external terminals and some of the internal circuitry. The types of regulators implemented will typically depend upon the polarity and amplitude of the voltage being regulated, relative to the power supply voltage applied to the device.

An example of a voltage regulator that is configurable as a charge pump voltage regulator or a negative polarity switching regulator is described in detail in copending application S.N. __/__, entitled "A Reconfigurable Topology for Switching and Charge Pump Negative Polarity Voltage Regulators", and filed contemporaneously and commonly assigned with this application, incorporated herein by this reference. Figure 4 illustrates a configurable voltage regulator according to this preferred embodiment of the invention.

Reconfigurable voltage regulator 128 is connected to external terminals of the integrated circuit, in similar manner as described above. In this example, external power supply terminal VCC receives the power supply voltage V_{cc} , in the conventional manner, and is connected to the drain of shared n-channel MOS transistor 81A in output driver 80. As will be described in detail below, output driver 80 is used in each of the charge pump and switching regulator modes. The source of MOS transistor 81A is connected to the drain of shared n-channel MOS transistor 81B. The gates of shared MOS transistors 81A, 81B are controlled by drive control circuit 83, and the body node of each of shared MOS transistors 81A, 81B are connected to their respective sources. Terminal DRV is connected to the node at the source of transistor 81A and the drain of transistor 81B, and terminal GND is connected to the source of transistor 81B. In typical configurations, terminal GND will be externally connected to ground potential.

N-channel MOS transistor 82A has its drain connected to the source of shared transistor 81B, at terminal GND, and has its source connected to terminal CP2. In turn, n-channel MOS transistor 82B has its drain connected to the source of transistor 82A, and its source connected to terminal SENS. The gates of MOS transistors 82A, 82B are connected to the pole of configuration switches 83A, 83B, respectively. As mentioned above, configuration switches 83A, 83B may be implemented in an appropriate manner for the particular technology of the integrated circuit; for example, CMOS pass transistors may be used to realize configuration switches 83A, 83B, in the case where the remainder of the integrated circuit is fabricated according to CMOS or BiCMOS technology. Each of configuration switches 83A, 83B are controlled, in this embodiment of the invention, by one or more bits in configuration register 85, which is writable under user or program control by other circuitry (not shown) in the integrated circuit. One throw of each of configuration switches 83A, 83B is connected to terminal GND. In switching regulator mode, configuration register 85 controls configuration switches 83A, 83B to connect the gates of transistors 82A, 82B to terminal GND, disabling these devices in that mode.

Conversely, configuration switches 83A, 83B operate to connect the gates of transistors 82A, 82B to drive control circuitry 88 in output driver 80 when voltage regulator 128 is in charge pump mode. Charge pump control circuitry 84 receives feedback inputs from respective throws of configuration switches 83A, 83B and from terminal SENS, and also receives a bandgap reference voltage from bandgap reference circuit 24. Charge pump control circuitry 84 issues a control signal, when enabled by configuration register 85, to drive control circuit 88 in output driver 80. Conversely, switching regulator control circuit 86 receives feedback inputs from terminals CP2 and SENS, and receives the bandgap reference voltage from bandgap reference circuit 24. When enabled by configuration register 85, switching regulator control circuit 86 issues control signals to drive control circuit 88 in output driver 80. Voltage regulator 128 also includes reference voltage generator circuit 87, which is connected to terminal REG, for use in switching regulator mode.

In operation, the selection of the operating mode of voltage regulator 128 is effected by the external connection of the appropriate devices to terminals DRV, CP2, SENS, and REG. In either mode, terminal VCC receives power supply voltage V_{cc} , and terminal GND is connected to system ground. Configuration register 85 is then written with the appropriate register word or bits that select the corresponding regulator mode. The writing of configuration register 85 may be carried out by the integrated circuit itself, for example under program control. Alternatively, configuration register 85 may be externally accessible, for example by way of a serial data terminal, to enable writing of configuration register 85 by the device user or the system within which voltage regulator 128 is implemented. Further in the alternative, in place of configuration register 85, logic circuitry may be provided that responds to a bias condition on a configuration terminal, such as described above relative to Figures 2, 3a and 3b.

Figure 5a illustrates an example of voltage regulator 128 as configured as a negative switching regulator. Switching p-channel MOS transistor 90 has its source biased to power supply voltage V_{cc} , and its gate connected to terminal DRV. The drain of transistor 90 is connected to passive network 92, which includes the appropriate network of an inductor, diode, and output capacitor, and resistor network, by way of which the output voltage at output terminal V_{out} is derived. A reference voltage generated by reference generator 87 is applied to the passive network from terminal REG, as shown. Feedback voltages at terminals CP2 and SENS are applied to switching regulator control 86, which in turn controls drive control circuit 88 and thus the current driven by switching transistor 90.

It is contemplated that those skilled in the art having reference to this specification will be readily able to construct the appropriate logic and circuitry involved in switching regulator control circuit 86. According to this preferred embodiment of the invention, switching regulator control circuit 86 includes an error amplifier that compares the voltage at terminal SENS against the bandgap reference voltage from bandgap voltage regulator circuit 24, and compares the error voltage against a triangle waveform at a configurable frequency, establishing a pulse width modulated control signal to output driver 80. In this example, output driver 80 operates as a non-inverting buffer,

so that the control signal effectively drives transistor 60 in a pulse-width modulated fashion. Additional circuitry may also be included within switching regulator control circuit 86, including a negative fault indicator that indicates when the regulator is not in regulation.

Additional detail regarding the construction and operation of switching regulator control circuit 86 is provided in the above-incorporated copending application S.N. / , , entitled "A Reconfigurable Topology for Switching and Charge Pump Negative Polarity Voltage Regulators".

Portions of the circuitry used in the charge pump regulator mode are disabled when voltage regulator 128 is configured as a switching regulator. In this example, configuration register 85 controls configuration switches 83A, 83B to connect the gates of transistors 82A, 82B, respectively, to ground potential at terminal GND, disabling those devices. Charge pump control circuitry 84 is also disabled by configuration register 85 in this mode, and conversely switching regulator control circuit 86 is enabled by configuration register 85.

Referring now to Figure 5b, the configuration of voltage regulator 128 as a charge pump regulator, according to this embodiment of the invention, will now be described. The external components include simply capacitor 94, which is a flyback capacitor connected across terminals DRV and CP2, and output capacitor 96, which is connected between terminal SENS, at which output terminal V_{out} is driven, and system ground. Terminal GND is connected to system ground, and terminal VCC is connected to power supply voltage V_{cc} ; terminal REG is simply not connected, as the reference voltage from reference generator 24 is not used in the charge pump configuration.

In this operating mode, configuration register 95 is written with the appropriate bits or data word to cause switches 83A, 83B to connect the gates of respective transistors 82A, 82B to drive control circuit 88 in output driver 80. Switching regulator control circuit 86 is disabled in this mode. Charge pump control circuit 84 includes the appropriate conventional circuitry for controlling the operation of voltage regulator 128 as a charge pump voltage regulator. In this example, charge pump control circuit 84

includes a comparator for comparing the output voltage at terminal SENS against a bandgap reference voltage from bandgap reference circuit 24, and for generating a control signal to drive control circuit 88 in output driver 80. Additionally, various level shift circuits are typically enabled in this example, so that the gate drive of the transistor pairs 81, 82 is at the proper level.

Additional detail regarding the construction and operation of charge pump control circuit 84 is provided in the above-incorporated copending application S.N. __/__, ____, entitled "A Reconfigurable Topology for Switching and Charge Pump Negative Polarity Voltage Regulators".

In operation, charge pump control circuit 84 issues a pulse width modulated signal to drive control circuit 88, which in turn applies the appropriate signals to the gates of transistors 81A, 81B, 82A, 82B. In charge pump fashion, transistor pairs 81, 82 cooperate to first charge flyback capacitor 94 to a positive voltage relative to ground by turning on transistors 81A, 82A and then, by turning on transistors 81B, 82B, applying this voltage as a negative voltage (below ground) to terminal SENS, considering that the voltage across capacitor 94 cannot instantaneously change. This negative voltage charges capacitor 96, and the process is repeated at the desired pulse width modulation rate, until the desired negative voltage at terminal SENS and thus at output terminal V_{out} is attained, at which point the modulation of transistors 81, 82 is adjusted accordingly.

According to the preferred embodiment of the invention, other features are also included within charge pump control circuit 84, including a negative fault indication function to indicate when voltage regulator 128 has not yet reached regulation, and circuitry responsive to configuration register 95 to select the desired regulated output voltage.

According to this embodiment of the invention, a configurable voltage regulator is provided, by way of which the voltage regulator can operate either as switching regulator or as a charge pump. In this embodiment of the invention, large output driver devices (e.g., transistors 81A, 81B) are used in both the charge pump and switching

regulator modes, enabling the implementation of both topologies of voltage regulator circuits in a configurable fashion within the same integrated circuit. In addition, this permits the integration of these output driver devices within the integrated circuit itself, reducing the number of external components required, especially for the charge pump topology in which only the external flyback and output capacitors are required. This particular configuration is also especially useful in generating a regulated negative polarity voltage, and as such this configuration may be included in the same integrated circuit as the configurable positive polarity voltage regulator described above, if desired.

GROUND OF REJECTION

The first ground of rejection is whether or not Claims 1 and 11 are unpatentable under 35 U.S.C. § 103 over Kanouda, secondly whether Claims 2 and 3 are unpatentable under 35 U.S.C. § 103 over Kanouda in view of Esteves; thirdly whether Claim 4 is unpatentable under 35 U.S.C. § 103 over Kanouda in view of Basso; and lastly whether or not Claim 12 is unpatentable under 35 U.S.C. § 103 over Kanouda in view of Matsuyama.

ARGUMENTS FOR THE REJECTION UNDER 35 U.S.C. § 103 OVER KANOUDA

It is respectfully submitted that Kanouda does not disclose or suggest the presently claimed invention including at least one configuration switch for selectively coupling elements of a feedback circuitry to the output drive circuitry responsive to the control signals from the configuration circuitry.

The Examiner alleges that elements 12, 13, and 52 disclose the configuration circuitry.

However, the Examiner's attention is directed to Kanouda in Figure 1 where these elements are connected to the input terminals of the main power switches 2, 3 and consequently not coupled to the output.

**ARGUMENTS FOR THE REJECTION UNDER 35 U.S.C. § 103 OVER KANOUDA IN
VIEW OF ESTEVES**

Additionally, it is respectfully submitted that Esteves does not disclose or suggest the presently claimed invention including at least one configuration switch for selectively coupling elements of a feedback circuitry to the output driver circuitry responsive to control signals from the configuration circuitry.

Again, Esteves discloses that the error amplifier 217 is connected to the logic 212 to drive the main switches 221 and 222.

Again, consequently this does not disclose the claimed subject matter.

**ARGUMENTS FOR THE REJECTION UNDER 35 U.S.C. § 103 OVER KANOUDA IN
VIEW OF BASSO**

Furthermore, where or not, Basso discloses a microcontroller to control the mode selection and whether or not one of ordinary skill in the art would consider modifying Kanouda is of no moment since the resulting construction would still in no way disclose or suggest the presently claimed invention.

**ARGUMENTS FOR THE REJECTION UNDER 35 U.S.C. § 103 OVER KANOUDA IN
VIEW OF MATSUYAMA**

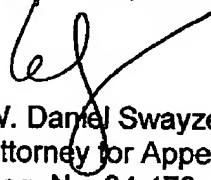
Additionally, whether Matsuyama discloses coupling two regulators together and whether or not one of ordinary skill in the art would consider modifying Kanouda is of no moment since the resulting construction would still in no way disclose or suggest the presently claimed invention.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-4, 11, and 12 under 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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APPENDIX

Claim 1 (previously presented): An integrated circuit, comprising:
a plurality of terminals including at least one output terminal and at least one input terminal; and

a configurable voltage regulator operable in a first mode or a second mode, comprising:

output driver circuitry, having an output terminal and an output coupled to said output terminal;

control circuitry, having an input terminal and at least one input coupled to said input terminal, having an output coupled to the output driver circuitry, and including a plurality of elements;

configuration circuitry, for receiving a configuration signal; and

at least one configuration switch, for selectably coupling elements of a feedback circuitry to the output driver circuitry responsive to control signals from the configuration circuitry.

Claim 2 (original): The integrated circuit of claim 1, wherein the configuration circuitry comprises:

a configuration amplifier, having a first input connected to the input terminal, and having a second input connected to a reference voltage, the configuration amplifier having an output coupled to the at least one configuration switch.

Claim 3 (original): The integrated circuit of claim 2, wherein the at least one configuration switch has first and second positions;

and wherein the at least one configuration switch is in the first position responsive to a voltage at the input terminal being above the reference voltage, and is in the second position responsive to a voltage at the input terminal being below the reference voltage.

Claim 4 (original): The integrated circuit of claim 1, wherein the configuration circuitry comprises:

a writable configuration register, coupled to the at least one configuration switch, for receiving and storing configuration data indicating the selected mode.

Claim 11 (original): The integrated circuit of claim 1, further comprising:
functional circuitry, coupled to the voltage regulator.

Claim 12 (original): The integrated circuit of claim 1, further comprising:
a second voltage regulator, having an output coupled to a second output terminal, for generating a negative polarity regulated voltage.

EVIDENCE APPENDIX

Appellants are submitting no items of evidence.

RELATED PROCEEDINGS APPENDIX

Appellants have no submission for the Related Proceeding Appendix.